Effective mobility of single-layer graphene transistors as a function of channel dimensions

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A detailed analysis of the extracted back gated FET mobility as a function of channel length, channel width, and underlying oxide thickness for both exfoliated and chemical vapor deposited (CVD) graphene is presented. The mobility increases with increasing channel length eventually saturating at a constant value for channel lengths of several micrometers. The length dependence is consistent with the transition from a ballistic to diffusive transport regime. The mobility as a function of channel width first increases and then decreases. The increase in mobility for very small channel widths is consistent with a reduction in edge scattering. The decrease in mobility for larger channel widths is observed to be strongly dependent on the oxide thickness suggesting that electrostatics associated with fringing fields is an important effect. This effect is further confirmed by a comparative analysis of the measured mobility of graphene devices with similar channel dimensions on oxides of different thicknesses. The observed electrical measurements are in excellent agreement with theoretical studies predicting the width dependence of conductivity and mobility. The mobility of CVD grown graphene is slightly lower than that of exfoliated graphene but shows similar trends with length and width. The mobility values reported in the literature are in agreement with the trend reported here. © *2011 American Institute of Physics*.
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I. INTRODUCTION

Graphene is a possible candidate for post CMOS applications and mobility is a material characteristic that has been utilized to gauge the material quality.[1] Numerous studies have been performed on the effect of temperature and dielectric types on graphene mobility. There are many papers reporting on the mobility of exfoliated graphene on SiO_2, graphene grown by CVD on Cu and by a precipitation process from Ni metal and transferred on SiO_2 with values ranging from about 2000 to about 25 000 cm^2/V s.[1–4] The large variation in mobility is typically attributed to factors such as scattering by defects in the underlying substrate,[5] residue from processing,[6] charged impurity and phonon scattering,[5–7] and substrate surface roughness.[8,9]

For semiconductor devices operating in the diffusive regime, mobility has been the parameter of choice for gauging and comparing device performance. One of the primary assumptions made is that the mobility is independent of channel dimensions. In this study, we performed room temperature effective mobility measurements as a function of channel dimension and graphene material source. The mobility exhibits a clear channel length and width dependence in both exfoliated and CVD grown graphene, with slightly lower mobilities for comparable channel dimensions on CVD graphene. The mobility varies from less than 1000 cm^2/V s to 7000 cm^2/V s depending on channel dimension. Theoretical analysis of the conductivity in graphene devices as a function of channel width performed by Vasko *et al.*[10] is in agreement with our experimental results. Mobility values for back gated devices with well defined channel dimensions in literature (exfoliated, CVD graphene grown on Cu and CVD graphene grown on Ni)[3,4,11,12] are seen to be consistent with the trend that we report here.

II. EXPERIMENT

Graphene for these experiments was obtained in two ways: (1) by mechanical exfoliation of natural graphite and (2) synthesized by chemical vapor deposition (CVD) on Cu with subsequent transfer to SiO_2/Si(100) substrates.[13] The single-layer graphene flakes from natural graphite were transferred onto a *p*-type Si wafer (doping $\sim 10^{17}/cm^3$) with thermal oxides of various thicknesses (15, 90, and 300 nm). The thermal SiO_2 was grown using a dry oxidation process. The growth process involved an initial growth of 5 nm oxide, followed by an etch in 100:1 buffered oxide etch (BOE), and subsequent growth of an oxide of the desired thickness. Monolayers of graphite on 90 and 300 nm SiO_2 were identified using optical microscopy and Raman spectroscopy.[14] For exfoliated graphene on 15 nm thermal oxide, monolayer

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flakes were identified and their thickness confirmed using scanning electron microscopy (SEM) and Raman spectroscopy, respectively. A standard two step electron beam lithography process was then used to etch the graphene flakes to desired dimensions and to define transfer length method (TLM) structures with channel lengths varying from 200 nm to 8 μm. The channel widths varied from 170 nm to 14 μm. Contact to the graphene transistors was made using nickel (60 nm) deposited at room temperature by electron beam evaporation at pressure at $\sim 10^{-7}$ Torr followed by a lift-off process in warm acetone (60 °C). The contact lengths were fixed at 1 μm and the contact widths were defined by the width of the graphene flake.

Graphene samples were synthesized by CVD on Cu as previously described.[13] The domain size of the graphene on Cu was varied by changing the pressure and flow rate of the methane gas and the furnace temperature.[13] The samples were characterized first by SEM to determine the surface coverage and then by Raman mapping after transfer to *p*-type Si wafers with 300 nm SiO_2. The transferred films were then used for device fabrication. The average domain sizes of the graphene films studied were about 6 and 20 μm.[15] Devices were fabricated using both standard photolithography as well as electron beam lithography (EBL). Because of the availability of much larger graphene films by the CVD process the channel lengths and widths were varied from 1 to 100 μm and 0.5 to 30 μm, respectively.

Hall and sheet resistance measurements were performed on CVD graphene films patterned and etched in the form of a Van der Pauw structure [inset, Fig. 1(b)].[16] The typical size of the graphene film was 10 by 10 μm. Ni contacts were deposited using electron beam evaporation, followed by wire bonding in a 16-pin DIP package to enable mounting to the cold finger of a cryocooler for variable temperature and magnetic-field measurements.

Electrical measurements were performed on back-gated field effect transistors at room temperature in air using a HP 4155 Semiconductor Parameter Analyzer and Cascade Probe Station. Low field Hall measurements were performed over the temperature range of 4–200 K, using a custom assembled Hall mobility apparatus incorporating a closed-cycle cryostat, ±1 T electromagnet, and Keithley/HP instrumentation.

III. RESULTS AND DISCUSSION

We performed a comparative analysis of three different mobility models to confirm that the observed trends in mobility described later in the paper were not a result of the extraction technique used. There are now primarily three techniques used for mobility extraction in graphene based devices. The Drude model which assumes a carrier concentration specific mobility determined using Eq. (2), where σ, n_{ind} and μ_{Drude} denote the conductivity, induced carrier concentration, and mobility respectively. For this model mobilities at high carrier concentration are typically reported.[1,17] The constant mobility model introduced by Kim *et al.*[18] assumes a carrier concentration independent mobility. The mobility using this model is determined by fitting the $R_{total} - V_{bg}$ curve with Eq. (3), where the contact resistance R_c, constant mobility μ_{const}, and charged impurity induced intrinsic carrier concentration n_0 are used as the variable parameters.[19] Here R_{total} is the total resistance of the device as defined by Eq. (3) below (which includes the contact resistance R_c), and V_{bg} is the back gate voltage on the

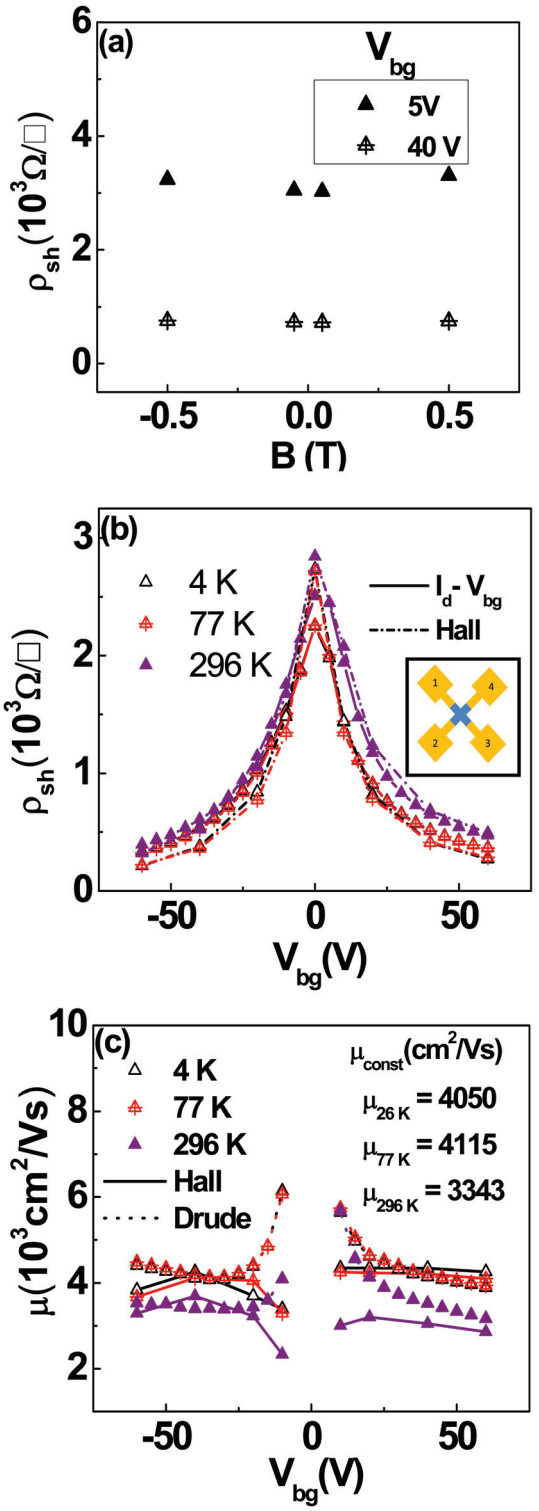

FIG. 1. (Color online) (a) Plot showing the variation of ρ_{sh} with magnetic field *B*. (b) Plot comparing the sheet resistance extracted from the constant mobility model and the sheet resistance from Van der Pauw measurements on the same film. (Inset) device structure. (c) Plot comparing effective mobilities extracted using the constant mobility model and the Drude model with the Hall mobility. All measurements were performed on the same CVD graphene film.

device. Finally, the third model proposed by Zhu *et al.*[7] assumes a carrier concentration dependent Hall mobility as given by Eq. (4) below.

$$n_{\text{ind}} = \frac{C_{\text{ox}} \cdot V_{bg}}{e}, \tag{1}$$

$$\sigma = n_{\text{ind}} \cdot e \cdot \mu_{\text{Drude}}, \tag{2}$$

$$R_{\text{total}} = 2R_c + \frac{L/W}{(\sqrt{n_0^2 + n_{\text{ind}}^2}) \cdot e \cdot \mu_{\text{const}}}, \tag{3}$$

$$\sigma_{xx} = n_{\text{ind}} \cdot e \cdot \mu_{\text{Hall}}. \tag{4}$$

The inset of Fig. 1(b) is a diagrammatic representation of the Van der Pauw (VDP) structure used.[16] All of the measurements were performed on the same graphene device. In the Van der Pauw arrangement, the Hall mobility was determined using the formula $\mu_{\text{Hall}} = 1/ne\rho_{\text{sh}}$. To rule out the possibility of the sheet resistance, ρ_{sh}, and hence the Hall mobility being affected by the application of a magnetic field, ρ_{sh} was determined as a function of magnetic field and the applied back-gate bias. The result of the analysis is shown in Fig. 1(a) where a very weak dependence of the ρ_{sh} on the applied magnetic field is observed. Mobility and sheet resistance values extracted using the constant mobility model were compared with mobilities from the Drude model and with mobility and sheet resistance values from Hall measurements. The comparison was also performed at three temperatures, 4, 77, and 296 K. The extracted sheet resistance from the constant mobility model [Fig. 1(b)] agrees well with the sheet resistance from Van der Pauw measurements on the same film. The mobility comparison is shown in Fig. 1(c). The trend observed for the variation of Hall mobility with temperature and induced carrier concentration is in agreement with the literature.[7] The extracted mobility from the constant mobility model, as a function of temperature is seen to correspond with the Drude model and Hall mobility at moderate and high back gate bias, which is the value typically reported in the literature.[6,7] For the rest of this paper, the mobility is extracted by using the constant mobility model. The difference in mobility at low back gate bias is attributed to the use of n_0 in the calculation of the total carrier concentration for the constant mobility model. The values of extracted intrinsic carrier conc.(n_0) were found to typically vary from $10^{11} - 5 \times 10^{11}$ cm^{-2} and $7 \times 10^{11} - 3 \times 10^{12}$ cm^{-2} for exfoliated and CVD graphene devices, respectively.

There have been theoretical and experimental studies reporting the effects of scattering by charged impurities from the underlying substrate (SiO_2 here) on the measured device characteristics. Effects of the underlying substrate include a limit of the maximum measurable mobility,[1,6,19,20] and a finite value of carrier concentration at the Dirac Point.[19] Device to device scatter in the measured mobilities have been attributed to charge inhomogeneities in the graphene sheet because of the underlying substrate (SiO_2).[21] Recently, several studies reported mobility values for top gated devices using both low-κ and high-κ gate dielectrics.[11,12,18,22] In these reports, the effect of the top gate dielectric on mobility was studied and compared to the case without a dielectric, i.e., mobility measurements with a back-bias only. The fundamental assumption made in this previous work is that the mobility does not vary as a function of channel dimensions.

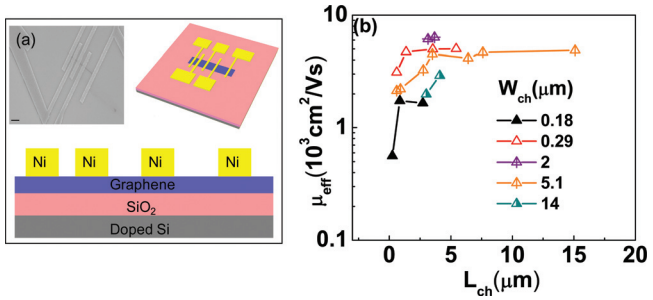

FIG. 2. (Color online) (a) SEM image, schematic of the top view and cross-section of a typical device structure used for the study (scale bar on SEM image is 2 μm). (b) Effective mobilities for devices on exfoliated graphene flakes, plotted as a function of channel length for different channel widths.

Figure 2(b) shows the extracted effective mobility as a function of channel length (L_{ch}) for given channel widths on exfoliated graphene. The mobility increases with increasing channel length and eventually saturates to a constant value at channel lengths of several micrometers. This trend has been previously reported, albeit using a different mobility extraction technique.[23] Previous work has suggested that the mean free path (l_{MFP}) in graphene is $\geq$200 nm (Ref. 21) and the observed trend is attributed to the device operating in both a quasiballistic regime and a diffusive regime, depending on the channel length.

Figure 3(b) compares the effective mobility (μ_{eff}) as a function of different widths for specific channel lengths. The mobility and the conductivity [Fig. 3(a)] first increases and then decreases as a function of channel width W_{ch}. For W_{ch} in the range of a few hundred nm, where $d/W_{\text{ch}} \geq 1$, we observed that the conductivity (from experiment) and mobility (from the fit) decrease with channel width (where d is dielectric thickness). Mobility degradation with decreasing width (W_{ch}) has been observed previously and explained in terms of edge scattering.[24]

The mobilities have a strong inverse dependence on the channel width, especially for widths greater than the thickness of the dielectric and are seen to saturate for large widths. Berger *et al.*[25] observed that mobility has an inverse dependence on W_{ch} and attributed it to possible inhibition of back-scattering; the issue of the channel length affecting the mobility as an independent parameter was however not observed/considered in that study. In this paper, we specifically addressed the effect of L_{ch} and W_{ch} on the mobility while keeping one of the parameters (W_{ch} or L_{ch}) constant. We now attempt to explain the observed inverse dependence.

Graphene on a dielectric behaves like a strip capacitor, with the dielectric thickness d (here $d = 300$ nm) and the plate width given by the device channel width W_{ch}. Nishiyama *et al.*,[26] showed that for any strip capacitor with $d/W_{\text{ch}} > 0.01$, fringing electric field lines cause accumulation of induced charge carriers along the edge of the channel. This results in an enhanced charge density distribution at the edges when compared to the rest of the channel. Charge accumulation at the edges was recently shown to theoretically occur for a narrow graphene strip (0.1 to 1 μm).[27]

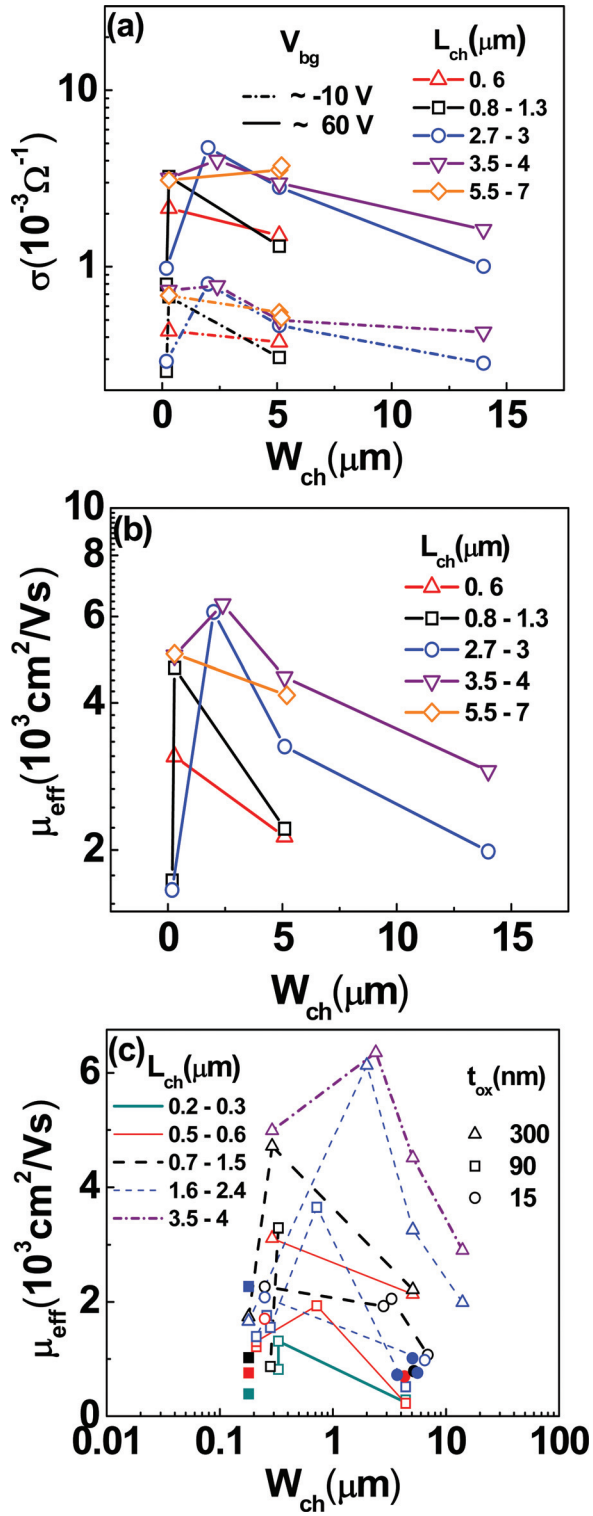

FIG. 3. (Color online) (a) Plot showing the channel conductivity as a function of channel dimensions. (b) Width dependence of effective mobility as a function of different channel lengths. (c) Effective mobilities for exfoliated graphene devices as a function of L_{ch}, W_{ch}, and dielectric thickness d.

Vasko *et al.*[10] theoretically showed that for a graphene strip 0.5 – 3 μm on 300 nm SiO_2, with the aspect ratio $d/W_{ch} < 1$ and $d > l_{MFP}$ in graphene, the charge accumulation results in an overall enhanced conductivity in the system, when compared to a system with uniform charge carrier distribution throughout the width of the channel. This charge redistribution is supposed to occur for any system that is in a strip capacitor configuration. The enhanced channel conductivity and extracted mobility is more obvious in a graphene based system, primarily because of the low carrier concentration.

To confirm that the underlying dielectric thickness does play a major role, we also performed an analysis wherein we compared the mobility values for exfoliated graphene devices of comparable channel lengths and widths but on thermal oxides of varying thicknesses, namely, 15, 90, and 300 nm. If our speculation regarding the mobility dependence on the aspect ratio (d/W_{ch}) is correct, then reducing the dielectric thickness d for a given L_{ch} and W_{ch} should have the same effect as increasing the W_{ch} for a given dielectric thickness. In other words, the mobility should reduce and saturate in the regime that is dominated by the redistribution of the charge carrier concentration, with decreasing d, but the edge scattering dominated degradation regime should remain. As we see in Fig. 3(c), when we reduce the thickness of the underlying dielectric from 300 to 90 to 15 nm, the mobility eventually decreases and saturates, until a minimal dependence on the channel width is observed. However, mobility degradation is observed for devices with channel widths of a few hundred nanometers. Thus, a given device has two parameters influencing the observed mobility, depending on W_{ch}, namely, edge scattering and enhanced charge distribution at the edges because of fringing fields. For channel widths of less than a few hundred nanometers, edge scattering plays a more significant role and hence leads to the observed mobility and conductivity degradation.

Figure 4(a) shows the ρ_{sh}–V_{bg} characteristics for an exfoliated graphene device and a CVD graphene device. CVD graphene devices exhibit a higher sheet resistance compared to exfoliated graphene; the difference is attributed to the presence of domain boundaries,[28] wrinkles, and residue from the transfer process. The R_{total} –V_{bg} characteristics were fitted using the model reported by Kim *et al.*[18] Figure 4(b) is a comprehensive plot showing the channel length and width dependence for exfoliated and CVD graphene, compared with mobility values for back gate bias measurements from the literature.[3,4,11,12] As seen in Fig. 4(b), a similar trend in terms of channel dimension dependence is observed in the case of synthesized graphene. For comparable channel lengths and

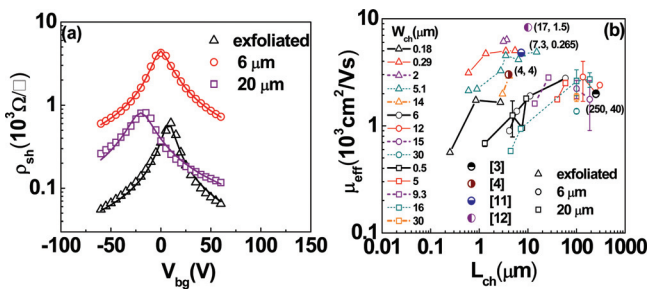

FIG. 4. (Color online) (a) Comparative plot showing the $\rho_{sh} - V_{bg}$ characteristics and corresponding mobility fits for exfoliated and CVD graphene samples. (b) Comprehensive plot showing the channel dimension dependence for back gated exfoliated and CVD graphene devices. Reported values from literature for measurements on exfoliated (Refs. 11 and 12) and CVD graphene grown on Cu[4] and Ni[3] are included for comparison. Coordinates indicate the device dimensions.

widths, the CVD graphene is seen to exhibit a lower mobility compared to exfoliated graphene, and a weak dependence on domain size is also observed. The observed scatter can be partially attributed to the variation in channel dimensions. The lower mobilities and dependence on domains is attributed to the presence of domain boundaries, wrinkles, and possible residue from the transfer and processing in the channel region. Data points from the literature are seen to be in agreement with the general trend shown in the plot. This leads us to strongly suggest that the previously overlooked channel dimension dependence is a major cause for the observed mobility scatter in back gate biased graphene devices.

IV. CONCLUSION

In summary, the mobility behavior in graphene devices was studied as a function of channel length and width. The extracted mobility in back gated graphene based devices was seen to exhibit channel dimension dependence. For a given channel width, the length dependence is attributed to the device operating in both the quasiballistic and the diffusive regimes, as previously reported.[23] For a given channel length, the mobility is seen to first increase and then decrease with channel width. The width dependence is partially attributed to edge scattering and partially to enhanced conductivity in the channel as a result of electrostatically induced charge accumulation along the edges. The charge accumulation is a result of the graphene on SiO_2 behaving as a strip capacitor. The channel dimension dependence was previously overlooked and is found to be a major contributing factor to the scatter in mobility values that have been reported. Similar trends were observed for the case of CVD graphene synthesized on Cu. For comparable channel lengths and widths, the CVD graphene was observed to have slightly lower mobilities than exfoliated graphene. This is attributed to defects in the graphene sheet (domain boundaries, wrinkles, and possible residue from the transfer process). Reported mobilities for back gate measurements from literature were seen be in agreement with the trend reported in this paper. Since mobility is an important parameter to gauge the performance of a graphene FET, a consistent way to measure and report the mobility value is necessary. A possible way to ensure measurement of meaningful mobility values would be the use of thin dielectrics either as the substrate of choice or as a top gate dielectric. This will effectively minimize the anomalous mobility values otherwise reported.

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