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Patterning silicon carbide on silicon by ion modification of C_{60} films

L. Moro, A. Paul, D.C. Lorents, R. Malhotra *, R.S. Ruoff, L. Jiang

Molecular Physics Laboratory, SRI International, 333 Ravenswood Avenue, Menlo Park, CA 94025, USA

Abstract

Reaction of C_{60} with Si at temperatures above 800°C is known to give SiC. Furthermore, treatment of vapor-deposited C_{60} films with a beam of Ar^+ transforms the surface layer of C_{60} into a nonvolatile carbon deposit. Based on these two findings, we have developed a method for patterning SiC structures on silicon. C_{60} is first vapor deposited onto a clean Si surface. By rastering the ion beam on selected parts of the sample, we write a chosen pattern on the C_{60} film. Upon increasing the temperature to around 300–350°C, the C_{60} film remains only in the areas that were subjected to irradiation, while it evaporates off the remaining surface. During the subsequent annealing at 900°C, the modified C_{60} layer confines the underlying C_{60} on the silicon surface, allowing the formation of SiC. At shorter times, traces of the capping layer are visible at the edges of the irradiated zone. These results demonstrate the principle of fabricating lithographically patterned SiC structures on silicon without masking and etching processes and with the high lateral resolution possible with ion beams.

1. Introduction

Silicon carbide has been proposed for many years as a material for microelectronics devices with special applications (high temperature, high power, high frequency) [1] and more recently for MEMC applications [2–4]. Among the physical characteristics which make this material particularly attractive are its wide band gap, which allows the material to be used as a high temperature semiconductor, its high thermal conductivity, and its chemical inertness, hardness and wear resistance.

The CVD growth of SiC films by carbonization of acetylene, propane or methane on silicon substrates, sometimes with an extra supply of silicon (by SiH_4 or SiH_2Cl_2 gases) has been reported [5–9]. These processes require a fairly high temperature (1000–1500°C).

Recently carbonization of Si by C_{60} has been proposed as a method to produce epitaxial β-SiC on silicon at a lower temperature (800–1000°C) [10]. Because C_{60} does not react with SiO_2 surfaces, the use of patterned Si/SiO_2 substrate has been suggested for selective growth of patterned SiC on Si. This approach has been followed by a few groups and the process for growing SiC have been described [11,12]. In all of these processes a beam of C_{60} impinges on the surface of a silicon substrate held at temperature of 800–1000°C.

Here we report a different approach which allows direct patterning of SiC structures on silicon substrates starting with a pre-deposited C_{60} film. The fabrication of submicrom SiC structures on silicon is demonstrated in a very simple process.

2. Results and discussion

This process for the fabrication of patterned SiC on Si is illustrated in Fig. 1. It begins with the deposition of a 200–300 nm thick C_{60} film on a Si substrate in a UHV chamber ($< 10^{-8}$ Torr). After deposition the C_{60} film is bombarded by an ion gun (Ar^+ or Ga^+ ions) in selected areas in order to create a non volatile layer which acts as a cap confining the remaining C_{60} molecules on the surface during the subsequent annealing at elevated temperatures.

A visible change in the C_{60} films is produced by ion irradiation. In this energy range the thickness of the ion modified region is about 10 nm; that is the penetration range of the primary ions in C_{60} according to TRIM simulations [13]. No change was seen upon varying the beam energy provided that it is higher than 2 keV. No difference was noted in this range (10^{15} and 10^{16} cm^{-2}) of irradiation dose. Preliminary Raman analysis of the modified film show a lower intensity of the C_{60} signal in the irradiated areas. In the same areas also the Si peak disappears or has a lower intensity, in agreement with what has been reported by other investigators [14].

Upon increasing the substrate temperature to 300–350°C, the C_{60} film evaporates off the un-irradiated surface, but it remains trapped on the surface under the modified C_{60} capping layer and reacts with Si to give SiC at 900°C for times longer than 150 min.

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* Corresponding author. Fax: + 1-415-859-6196.

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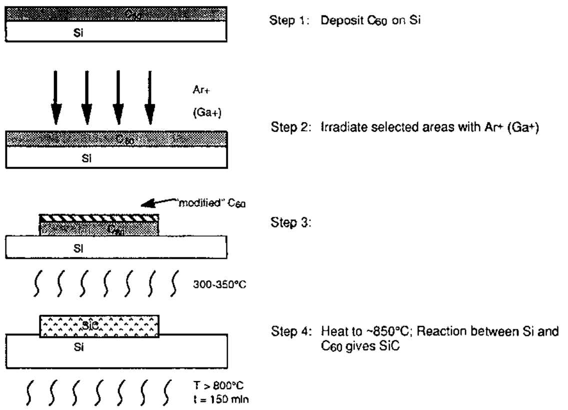

Fig. 1. Four steps of forming patterned SiC on Si.

Even after 150 min at 900°C, the carbidization reaction is not complete throughout the thickness of the C_{60} film. The partially converted film and the capping layer, which have a substantial thermal and lattice mismatches with the silicon substrate, break because of the stress produced by heating up and cooling down the sample for annealing. SEM observations of the film reveal the wrinkles and cracking in the film as well as the underlying pits produced on the silicon substrate by the depletion of Si atoms migrating to react with C_{60} and form SiC.

2.1. Evidence for carbide formation

For longer annealing time (300 min), the reaction between C_{60} and Si is complete with the formation of a layer of silicon carbide. FTIR analysis of the film showed a band at 796 cm^{-1} corresponding to Si–C bonds in silicon carbide. Formation of SiC was further confirmed by Auger analysis which showed characteristic line shape for SiC (C_{KLL} at 275 eV and shoulder at 264 eV; Si_{LVV} at 94 eV and an absence of a shoulder at 88 eV). The crystalline nature of the SiC layer formed at 900°C, 300 min has been detected by preliminary TEM analyses. The quality of the "ion modified" sample is very acceptable and has a grain size of approx. 40 nm.

The substrate orientation ((100) versus (111)) does not seem to affect the formation of the SiC film. Only the shape of the pits on the silicon substrate changes from square/rectangular to triangular. However, the formation of silicon carbide seems to be inhibited on amorphous silicon surfaces. On the surface outside the bombarded areas, a very thin layer of silicon carbide is formed in the early stages of the heating up process. This layer can be removed by a suitable chemical etch for SiC.

2.2. Lateral resolution

To demonstrate the lateral resolution achievable with this technique, we used a high-resolution liquid-metal (LM) Ga-ion gun. Comparison of high magnification optical microscope photos of the strips taken before and after annealing show no loss of resolution during the annealing process. This test also showed the feasibility of drawing SiC features on silicon having the resolution of the ion beam (< 1 μm).

In this small size Ga^+ patterns no thermally induced cracking or depletion pits were observed. As a matter of fact it is well known in microelectronics processing that in small features the mechanical stress is more easily released. On the other hand in presence of larger areas of bare silicon the major source of silicon atoms for the formation of SiC is provided by surface diffusion rather than by the slow diffusion process through the already formed SiC layer. Because of this major role played by the lateral surface diffusion, the largest size SiC grains are located at the edges of the patterned strips.

3. Conclusion

To summarize, our experiments have proved that SiC can be produced from pre-deposited C_{60} films on silicon by annealing at 900°C for $t > 150$ min. When the C_{60} pre-deposited film covers larger areas, the Si necessary for the reaction diffuses through the already formed SiC layer preferentially at defect sites in the films (e.g. grain boundaries). In the silicon substrate these preferential diffusion paths lead to pit formation in accord with previous literature reports [9–11].

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