Three-Gigahertz Graphene Frequency Doubler on Quartz Operating Beyond the Transit Frequency

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***Abstract*—We demonstrate a 500-nm graphene frequency doubler with a record 3-GHz bandwidth, exceeding the device transit frequency by 50%, a previously unobserved result in graphene, indicating that graphene multiplier devices might be useful beyond their transit frequency. The maximum conversion gain of graphene ambipolar frequency doublers is determined to approach a near lossless value in the quantum capacitance limit. In addition, the experimental performance of graphene transistor frequency detectors is demonstrated, showing responsivity of 25.2 μA/μW. The high-frequency performance of these gigahertz devices is enabled by top-gate device fabrication using synthesized graphene transferred onto low capacitance, atomically smooth quartz substrates, affording carrier mobilities as high as 5000 cm^2/V·s.**

***Index Terms*—Bandwidth, doubler, graphene, quartz, radio frequency devices, transit frequency.**

I. Introduction

GRAPHENE, a 2-D sheet of carbon atoms arranged in a honeycomb lattice [1], has attracted significant interest as a channel material for high-frequency analog electronics [2]–[14]. This can be attributed to its high-carrier mobility [15], large current densities [16], thermal and mechanical stability [17], [18] and intrinsic ambipolar electron–hole symmetry. A unique device application of its ambipolar property is for frequency translation where input signal frequencies can be translated up to higher frequencies (frequency multipliers) often in integer multiples or translated down to zero or baseband frequencies (frequency detectors) [2]–[5]. In recent years, frequency multipliers have received renewed attention particularly for terahertz (~100 GHz–1 THz) applications driven by strategic interests in security, imaging, short-range communication, and molecular spectroscopy [19].

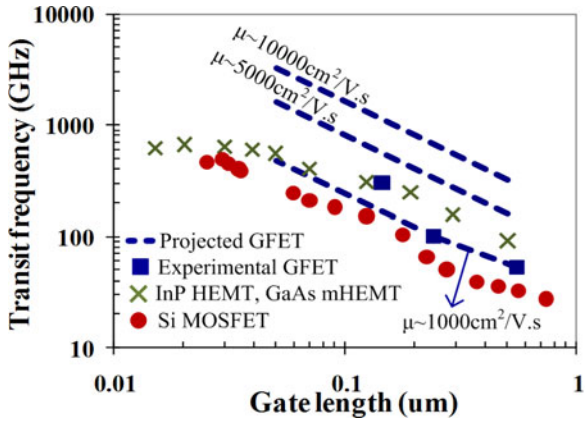

Fig. 1. Transit frequency comparison for different high-frequency FETs versus gate length. The symbols are experimental data points and the dashed lines are the projected mobility-scaled performance of GFETs. 300 GHz f_t is the fastest experimental GFET to date [10]. For terahertz operation, higher mobility scaled GFETs (dashed lines) offer the greatest prospects at moderate gate lengths. Figure adapted from Schwierz [11]. THz f_t values are also confirmed by quantum mechanical simulations that include velocity saturation [20].

Graphene field-effect transistors (GFETs) appear to be the most promising transistor device for terahertz applications owing to their high mobility which yields the highest cutoff or transit frequencies beyond the reach of conventional solid-state transistors as shown in Fig. 1. In this paper, we demonstrate for the first time a GFET operating ~50% beyond its transit frequency f_t. This previously unobserved result indicates that graphene devices employing the ambipolar property might be even more useful for high-frequency electronics than previously thought, potentially providing useful electronic performance beyond the experimental 300 GHz and predicted terahertz device transit frequencies [10], [20].

The fabricated GFET with 500-nm channel length and biased at the Dirac point for frequency doubling achieves a maximum output power of approx. −23.3 dBm and record bandwidth of 3 GHz, 2× higher than the state-of-the-art GFET frequency doubler [2]. The 3-GHz frequency bandwidth exceeds the measured 2-GHz device f_t by 50%, a new achievement for graphene devices. Operation beyond f_t is not entirely unexpected since the graphene frequency multiplier offers no gain. Nonetheless, this is the first experimental observation of graphene circuit

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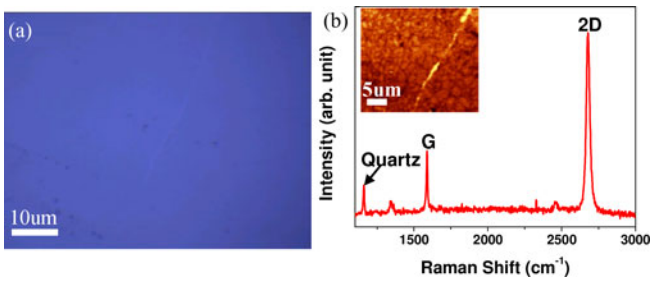

Fig. 2. (a) Optical image of graphene on quartz showing an even color indicative of uniform coverage. (b) Raman spectroscopy of the CVD grown graphene used in this work confirming the monolayer structure. *Inset:* Local Raman map of the unique monolayer 2-D peak showing uniform graphene coverage over 700 μm^2 area that enabled the fabrication of arrays of devices.

bandwidth exceeding the device transit frequency. The 3-GHz multiplier bandwidth is afforded by transferring CVD-grown graphene onto low capacitance, atomically smooth quartz substrates which is an ideal choice for low loss and temperature stable high-frequency electronics [21]. GFET carrier mobilities as high as ~5000 cm^2/V·s were observed, but can be as low as ~500 cm^2/V·s due to the resist residue of current solution-based transfer methods which lead to uncontrolled impurity and defect scattering [22], [23] as indicated by a relatively flat mobility–temperature profile [24], [25]. We have included supplementary downloadable material, which includes temperature dependent mobility data. Remarkably, even with a low mobility GFET, record gigahertz performance is achieved.

Furthermore, we address the most pressing question regarding the maximum conversion gain of GFET ambipolar frequency multipliers, uncovering an upper limit of near lossless frequency doubling in the quantum capacitance limit. In addition, the experimental performance of GFET frequency detectors was evaluated, showing current responsivity ($\Delta I_D/\Delta P_{\rm in}$) of ~25.2 μA/mW. The results reported here collectively indicate that optimized GFETs can enable high performance GHz and future terahertz systems via frequency translation and processing, an area of growing significance.

II. Device Fabrication and Performance

A. Graphene Synthesis

Large-area graphene films were synthesized on Cu substrates using a low-pressure CVD process as in [26]. After growth, the graphene was transferred to a single-crystal ST-cut quartz wafer by the process described in [27]. Fig. 2(a) shows an optical image of the monolayer graphene that has been transferred onto quartz, where the even color is indicative of uniform graphene coverage. As shown in Fig. 2(b), the Raman spectrum of the transferred graphene reveals a 2D peak at 2679 cm^{-1} with a full width at half maximum (FWHM) ~24.5 cm^{-1}, indicating monolayer graphene [28]–[30]. A peak at ~1160 cm^{-1}, due to the quartz substrate, is also observed [31]. The inset of Fig. 2(b) shows the Raman mapping corresponding to the intensity of the 2-D peak, which further validates the uniformity of the graphene film over a 700 μm^2 area, enabling the fabrication of arrays of devices.

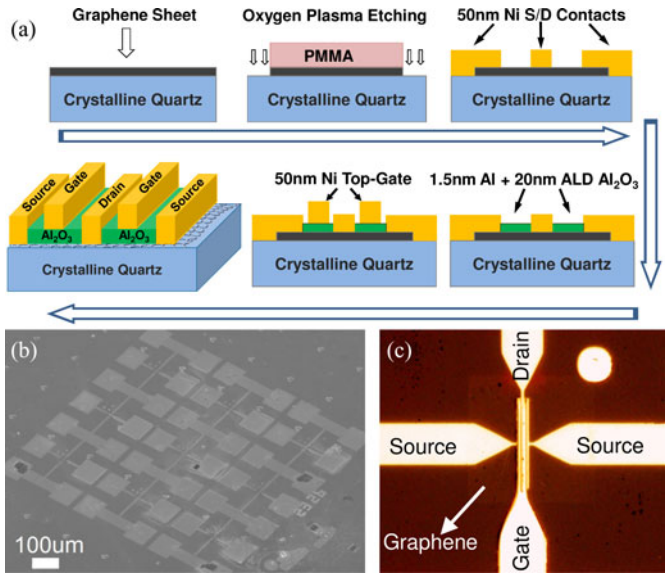

Fig. 3. (a) Illustration of top-gated graphene device fabrication process. (b) SEM image of a completed 3 × 3 array of GFETs fabricated with the process illustrated in (a). (c) Optical image of a typical GFET from the 3 × 3 array with an arrow indicating the location of a patterned graphene sheet underneath the active device region.

B. Graphene Transistor Fabrication

GFETs were fabricated as illustrated in Fig. 3(a) using electron-beam lithography (EBL) and standard cleanroom processes. Charging effects of the insulating quartz substrate during EBL processing were avoided by using a water-soluble conducting polymer (Espacer 300Z from Showa Denko K.K.). After transfer of the graphene to the quartz substrate, an active region was defined by EBL and oxygen plasma etching. A second EBL step was performed to define metal contacts for the source and drain of a ground-signal-ground (GSG) structure, followed by a 50-nm thick Ni e-beam evaporation and lift-off process. The gate dielectric consists of a 1.5-nm thick Al nucleation layer, followed by a 20-nm thick Al_2O_3 layer deposited by atomic layer deposition (ALD) [32]. A 50-nm thick Ni gate contact is then defined by EBL and a lift-off process. Fig. 3(b) shows a scanning electron microscope (SEM) image of a completed 3 × 3 array of GFETs fabricated by the process illustrated in Fig. 3(a), and Fig. 3(c) shows an optical microscope image of a typical GFET. The arrow indicates the location of the patterned graphene sheet underneath the active device region. DC and RF characterizations were performed using an Agilent Semiconductor Device Analyzer and Microwave Network Analyzer, respectively.

C. Device Performance

A representative transfer curve of a high-performance GFET on quartz is shown in Fig. 4 with extracted electron mobility of ~5000 cm^2/V·s, using a well-established low-field diffusive transport model [32], [33]. The high-mobility suggests electrically good quality graphene that is not substantially impacted by the complex device fabrication. The output characteristics of a GFET for frequency multiplication is shown in

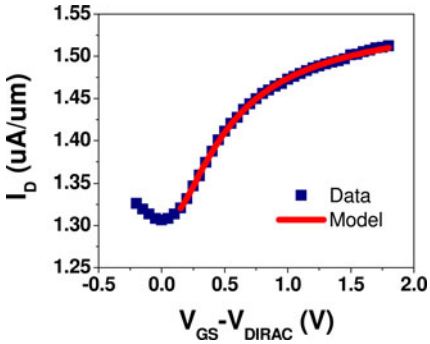

Fig. 4. Transfer curve of a GFET on quartz with 280 nm channel length. The electron mobility is ~5000 $cm^2/V{\cdot}s$ at room temperature in air extracted from a well-established low-field diffusive transport model [32], [33] ($V_{DS} = 10$ mV).

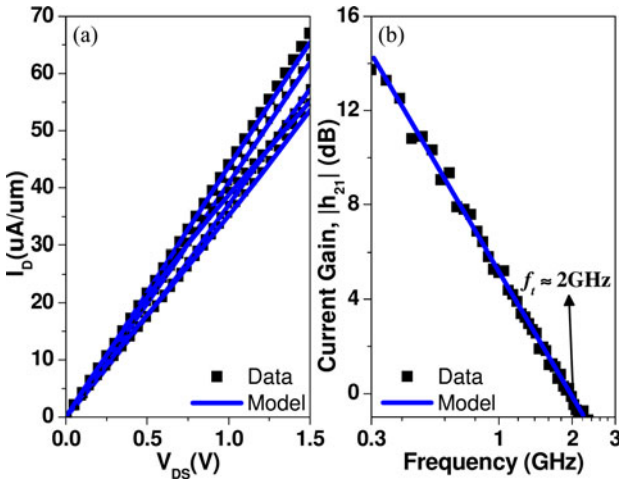

Fig. 5. (a) Output characteristics of the GFET multiplier in good agreement with a compact model based on prior work [34], [35]. V_{GS} varies from 0–2 V in 0.5 V steps. The validated compact model including nonidealities enables device and circuit performance assessment. (b) Measurement of the current gain of the GFET multiplier. The measured f_t is ~2 GHz including all the device intrinsic and extrinsic capacitances ($V_{DS} = 2.5$ V and $W/L = 50\,\mu$m/0.5 μm).

Fig. 5(a), in good agreement with a circuit model based on validated graphene compact models [34], [35]. The short circuit current gain $|h_{21}|$ of a ~500 $cm^2/V{\cdot}s$ mobility GFET is shown in Fig. 5(b). The device transit frequency f_t, including the effects of all capacitances and contact resistance R_c, was directly measured to be 2 GHz at the peak electron transconductance ($g_m \sim 13.4\,\mu S/\mu m$ at $V_{GS} \sim 2$ V) with $V_{DS} = 2.5$ V. The transit frequency can also be calculated as $f_t = g_m/(2\pi C_{ox})$ [3], [7], [11], where the gate oxide capacitance C_{ox} is ~190 nF/cm^2, based on the transistor dimensions ($W/L = 50\,\mu$m/0.5 μm) and the gate dielectric stack [7], [36]. Using this equation, f_t is calculated to be ~2.25 GHz, in close agreement with the measured value, indicating the weak effect of parasitic substrate and fringe capacitances, a direct benefit of using insulating quartz for high-frequency applications. Mobility improvements via robust nondetrimental graphene postgrowth transfer will proportionately increase the device speed. For example, a mobility of 10 000 $cm^2/V{\cdot}s$ for the given GFET will result in an f_t ~40 GHz. This is remarkable because of the high extrinsic f_t which is actually accessible for circuits, in contrast to the often reported intrinsic f_t which is an idealized metric. The maximum oscillation frequency f_{max} was also measured (not shown) to be ~1.8 GHz.

III. GFET Frequency Doubler

A. Experimental Performance

Fig. 6(a) shows the circuit schematic of a GFET frequency doubler, and Fig. 6(b) is the oscilloscope display, with clear evidence that the output (2 MHz) is oscillating at twice the input frequency (1 MHz). The device is biased at the Dirac point for maximum frequency doubling based on the intrinsic electron–hole symmetry [2]–[5]. The spectrum analyzer output shown in Fig. 6(c) confirms frequency doubling for an input frequency of 10 MHz and also illustrates the high spectral purity of the output signal for the GFET doubler, where more than 90% of the output power is at the doubled frequency. All other harmonics are $\geq 10\times$ lower. Fig. 7(a) shows the output power of the doubled signal with a measured small-signal slope ~20 dB/decade, as expected of ideal square-law ambipolar devices. Fig. 7(b) is the conversion gain ($P_{out,2f}/P_{in,1f}$, where $P_{in,1f}$ and $P_{out,2f}$ are the input and output powers at the fundamental and doubled frequency, respectively) of the GFET frequency doubler. Both the output power and conversion gain are in strong agreement with the compact circuit model, revealing up to −23 dBm of available power.

A primary metric for analog circuits is the −3-dB frequency (f_{-3dB}), which represents the actual frequency bandwidth in practical circuit implementations. The GFET doubler's frequency response presented in Fig. 8 reveals $f_{-3dB} = 3$ GHz, the highest bandwidth achieved for GFET frequency multipliers. The bandwidth, presently limited by low mobilities and contact resistance is expected to be at least $10\times$ higher in the intrinsic limit based on reports of a similar experimental GFET with 500-nm channel length [7].

B. Maximum Theoretical Conversion Gain

The conversion gain and output power of the GFET frequency doubler are presently limited by R_c, which is extracted to be ~290 Ω, on the order of the channel resistance at the Dirac point ($R_{Dirac} = 317\ \Omega$). The same graphene transistor with negligible contact resistance can provide a $10\times$ improvement in the conversion gain [see Fig. 9(a)]. We employ our validated circuit model to determine the maximum conversion gain achievable, currently the most pressing question related to graphene ambipolar frequency multipliers. In the theoretical limit of an ideal GFET with: 1) vanishing R_c and impurity carriers, 2) perfect electron-hole symmetry, and 3) saturation velocity bounded by the Fermi velocity (~10^8 cm/s), the maximum conversion gain approaches a near lossless (~−1.5 dB) performance as the gate oxide capacitance C_{ox} is scaled into the quantum capacitance C_q regime ($C_{ox} \gg C_q$) as shown in Fig. 9(b). This indicates that a $1000\times$ improvement is possible compared to existing

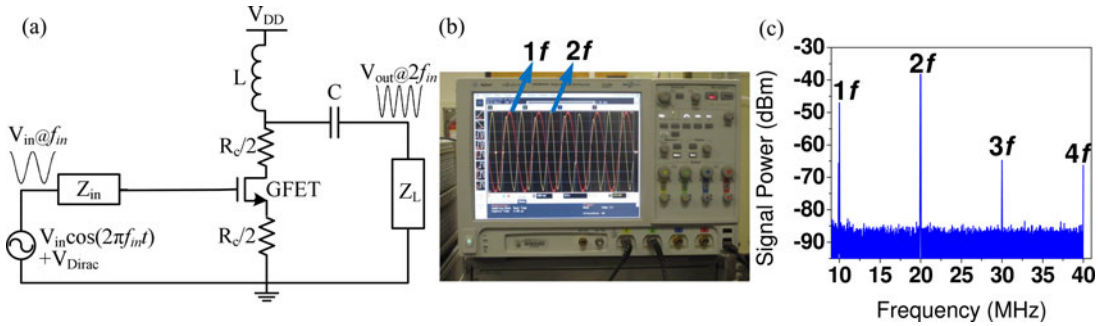

Fig. 6. (a) Circuit schematic of the GFET frequency doubler. $Z_{\rm in} = Z_L = 50\ \Omega$, typical of gigahertz and terahertz systems. For maximum frequency doubling based on electron-hole symmetry, the device is biased at the Dirac point. The L and C network are necessary to route the dc and ac signals separately at the output. (b) Real-time oscilloscope output showing GFET frequency doubling at 2 MHz. (c) Spectrum analyzer output with 10 MHz input frequency and 0 dBm power. More than 90% of the output power is at the doubled frequency. All other harmonics are more than 10× lower than the doubled signal.

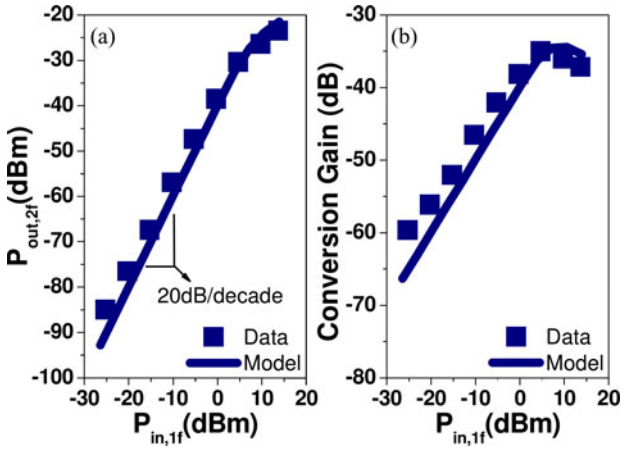

Fig. 7. (a) Doubled output power and (b) conversion gain of the experimental GFET frequency doubler with good agreement to graphene circuit model. The small-signal slope is 20 dB/decade expected of ideal square-law ambipolar devices. The GFET is biased at $V_{\rm DIRAC} = 1.4$ V and $V_{\rm DS} = 2$ V. The input frequency is 10 MHz and device $W/L = 50\ \mu$m/0.5 μm.

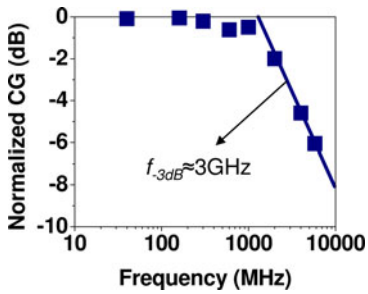

Fig. 8. Measured frequency response of the normalized conversion gain (CG) of the GFET frequency doubler. The straight line is the standard Bode guide for extracting the bandwidth. The extracted bandwidth is 3 GHz, a record bandwidth for GFET frequency multipliers. The GFET is biased at $V_{\rm DIRAC} = 1.4$ V and $V_{\rm DS} = 2$ V and device $W/L = 50\ \mu$m/0.5 μm.

experimental achievements in 50 Ω systems, and motivates the need for significant further device research and fabrication optimization. To place these results in perspective, the near lossless frequency doubling is >2× higher than an ideal varistor doubler, and comparable to an ideal varactor doubler, albeit without the inherent narrowband limitation of varactors.

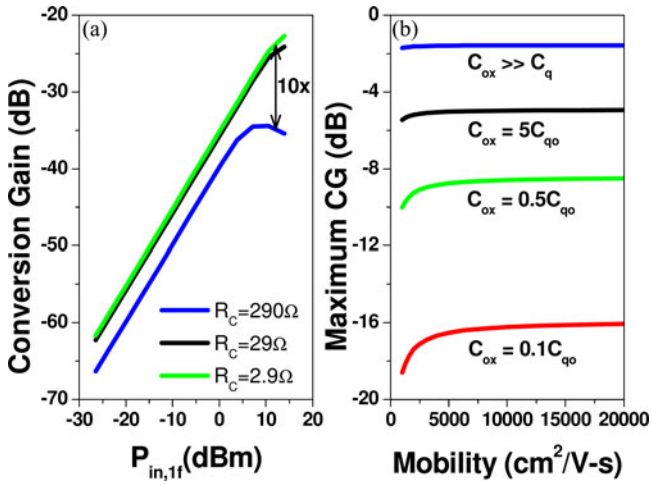

Fig. 9. (a) The simulated impact of R_c on the conversion gain of the experimental GFET frequency doubler. Circuit simulations indicate about 10× improvement in the maximum conversion gain if R_c were negligible compared to the channel resistance. For the experimental GFET, $R_c \sim 290\ \Omega$ and the channel resistance is ∼317 Ω. (b) Circuit simulations of the maximum conversion gain of an ideal GFET frequency doubler with scaled mobility and oxide capacitance revealing near lossless conversion gain in the quantum capacitance limit ($C_{\rm ox} \gg C_q$). $C_{\rm qo}$ (∼8.4 fF/μm^2) is graphene's equilibrium quantum capacitance, a useful reference for normalizing $C_{\rm ox}$.

IV. Experimental GFET Detector Responsivity

The current responsivity ($\Delta I_D/\Delta P_{{\rm in},1f}$) or sensitivity of the GFET to input RF signals is reported in Fig. 10(a). The responsivity, a key metric for frequency detector and direct-conversion wireless receivers is measured to be ∼25.2 μA/mW. Simulated removal of R_c results in >5× improvement of the responsivity [see Fig. 10(b)].

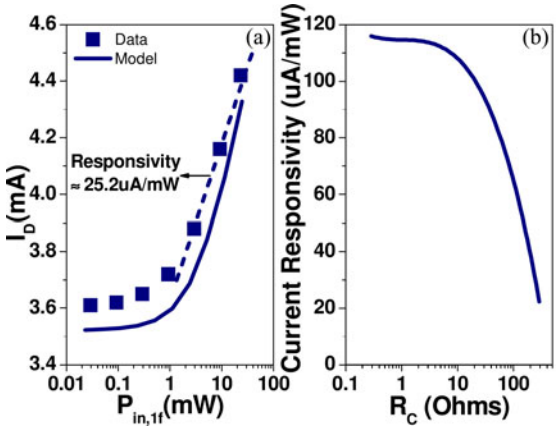

Fig. 10. (a) Experimental GFET detector responsivity ($\Delta I_D/\Delta P_{\mathrm{in},1f}$) measured for the first time. The input frequency is 10 MHz and the GFET is biased at the Dirac point for maximum rectification of ac signals. The dashed line is a visual guide. (b) Circuit simulation of the performance benefits available by minimizing contact resistance. The responsivity improves by more than 5× by scaling down R_c from 290 Ω to values much smaller than the channel resistance (∼317 Ω).

V. Conclusion

In summary, a record 3-GHz experimental graphene frequency doubler employing the intrinsic electron-hole symmetry has been reported on low capacitance, smooth crystalline quartz substrates. The 3-GHz operating bandwidth exceeds the device f_t by 50%, indicating that graphene multiplier circuits can substantially exceed the device transit frequency. In the limit of vanishing device nonidealities, we uncovered that near lossless frequency multiplication is possible, making optimized GFETs an attractive device for frequency multiplication at sub-THz frequencies beyond the frequency capability of conventional solid-state FETs.

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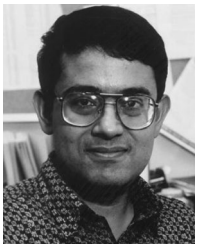

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